4. (Amended) A semiconductor device comprising:

a plurality of wiring lines which are formed of Cu whose concentration is equal to or higher than 10^{19} atoms/cm^3; and

an insulating layer which has a property that Cu is unlikely to enter said insulating layer and which insulates between said plurality of wiring lines; and

at least one adhesion layer formed in an interface between said plurality of wiring lines and said insulating layer, said at least one adhesion layer allowing said plurality of wiring lines and said insulating layer to adhere to one another, wherein said at least one adhesion layer has an etching rate which is essentially equivalent to an etching rate of said plurality of wiring lines,

wherein each of said at least one adhesion layer has a polishing rate which is essentially equivalent to a polishing rate of said plurality of wiring lines.

REMARKS

Attached hereto is a marked up version of the changes made in the claims by the current Amendment. The attached page is captioned "**Version with markings to show changes made.**"

It is noted that the claim amendments herein are intended solely to more particularly point out the present invention for the Examiner, and not for distinguishing over the prior art or the statutory requirements directed to patentability. It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.